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Gated Photocathode Design for the P510 Electron Tube used in the National Ignition Facility (NIF) Optical Streak Cameras

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ABSTRACT

The optical streak cameras currently used at the National Ignition Facility (NIF) implement the P510 electron tube from Photonis¹. The existing high voltage electronics provide DC bias voltages to the cathode, slot, and focusing electrodes. The sweep deflection plates are driven by a ramp voltage. This configuration has been very successful for the majority of measurements required at NIF. New experiments require that the photocathode be gated or blanked to reduce the effects of undesirable scattered light competing with low light level experimental data. The required ~2500V gate voltage is applied between the photocathode and the slot electrode in response to an external trigger to allow the electrons to flow. Otherwise the slot electrode is held approximately 100 Volts more negative than the potential of the photocathode, preventing electron flow. This article reviews the implementation and performance of the gating circuit that applies an electronic gate to the photocathode with a nominal 50ns rise and fall time, and a pulse width between 50ns and 2000ns.

Key Words: Streak Camera, Gated Photocathode, Streak Tube, Push-Pull MOSFET Gate Topology, High side gated cathode

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1. INTRODUCTION

The National Ignition Facility (NIF) is a 192 laser beam facility designed to support the Inertial Confinement Fusion (ICF) and High Energy Density (HED) programs to name a few. Several experimental systems have been built to support a variety of complex measurements using an optical streak camera system. These systems measure the high-speed temporal response of light emanating from the plasma after the target has been intercepted by the main laser beams. When the camera is coupled to a spectrometer system, the temporal response as a function of wavelength can be measured. Coupling the streak camera to an interferometer system allows for complex velocities to be measured during the laser plasma interactions. All the optical streak camera systems used at NIF are currently designed around the sealed P510 tube from Photonis¹. The camera is a sealed electron tube integrated with an optical module that delivers light to the photo-cathode and a scientific grade CCD that interfaces to the phosphor window at the rear of the tube.

The typical implementation of the sealed optical streak tube uses several DC voltages to establish proper functionality of the device. This includes the cathode, slot and focus voltages. Also this implementation includes sweep plates that are driven by the action of a linear ramp generator. The DC voltage on the cathode is held at the lowest potential referenced to the anode ground (phosphor window). The DC slot voltage is defined with respect to the cathode voltage to have approximately 2500 Volt difference. The DC focus voltage is based on the final electron energy exiting the slot electrode such that the electrons come to best focus at the phosphor plane. The electrical DC bias configuration of the tube is shown in figure [1].

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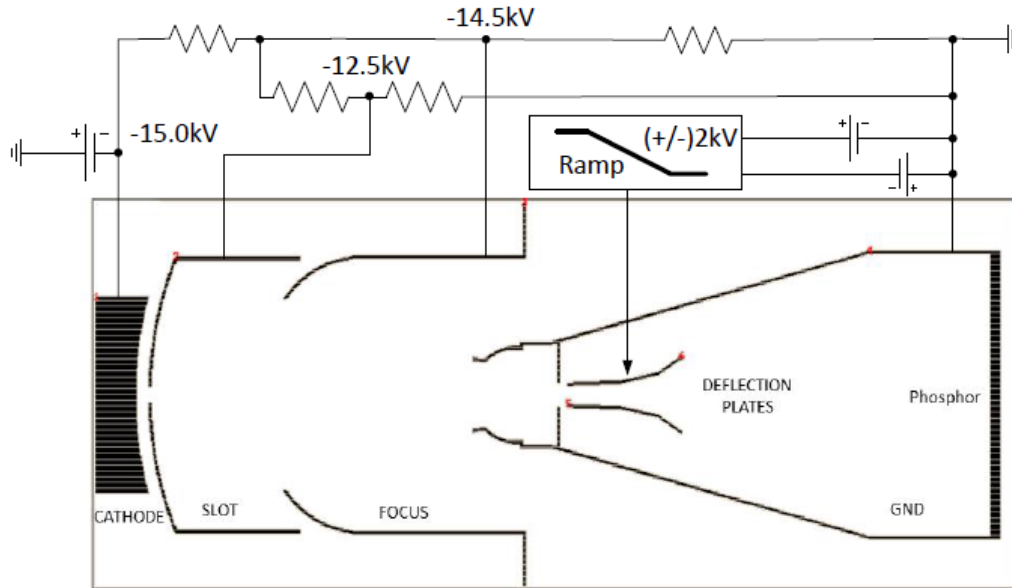


Figure [1] shows the electrical DC bias implementation for the standard P510 tube configuration. The bias voltages are nominal values and can slightly differ for each tube. For this DC configuration the cathode is set to (-15kV), the slot is set to (-12.5kV) and the focus is set to (-14.5kV). The sweep voltages when triggered traverse between (+2kV and -2kV) where the rate of transition defines the time window of the acquisition.

Figure 2 shows the electron trajectories for a conventional implementation of the P510 tube2 and biased as described in figure [1]. The sweep voltages are set equal to zero for this plot limiting the electron flow to the horizontal axis.

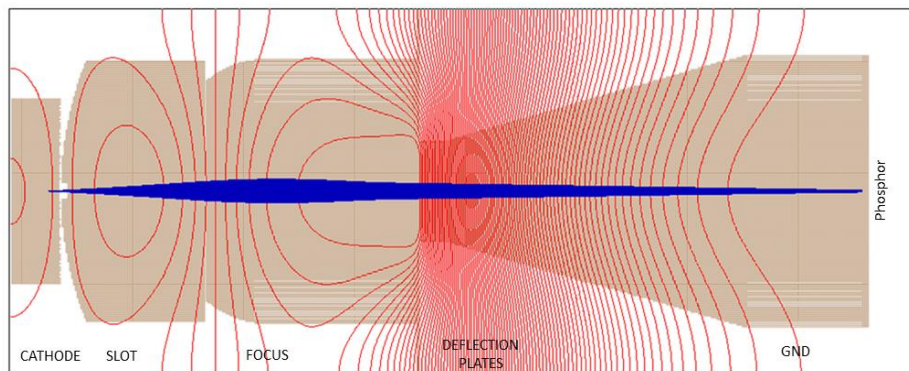


Figure [2] is an electron flow diagram for the P510 streak tube at the nominal DC operating voltages. The voltages are Cathode (-15kV), Slot (-12.5kV), and the Focus (-14.5kV). The sweep deflection plates have a nominal ramp voltage of (+/-2kV), and for this plot are set to have equal voltages (zero) limiting the electron flow to the horizontal axis. The cathode and slot extraction electrode are both sized at 0.5mm.

When the tube is integrated with an electronic controller and a charge coupled device (CCD) to read out the data from the 2D phosphor, various time-resolved measurements can be made over a broad wavelength band. The wavelength band is determined by the choice of photocathode material. For the NIF, the two cathode materials are the S1 and S20 which

cover the bands of (300-1200) nm and (300-850) nm respectively. Figure [3] describes a typical streak camera arrangement.

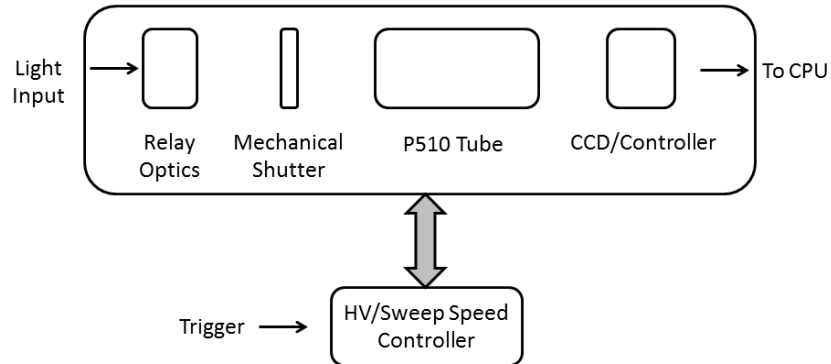


Figure [3] describes the major components of the optical streak camera. The camera includes relay optics, mechanical shutter, sealed streak tube, CCD, and electronics that support HV bias controls, ramp driver and low voltage control logic.

This article discusses the implementation of a tube gating capability designed to pulse the extraction slot electrode prior to the initiation of the ramp voltages which determines the sweep window. The slot voltage floats on the negative 15kV supply and is pulsed to a positive 2.5kV having a final voltage equivalent to the DC operating voltage of negative 12.5kV. The pulse is on for the duration of the sweep and only after the sweep has completed is the pulse turned off to prevent signal from being recorded during the retrace of the ramp circuit. This type of gating blocks the flow of electrons from the cathode prior to and after the sweep occurs on the nanosecond time scales. This also eliminates the need for a mechanical shutter and eliminates data corruption that is observed with retrace effects. Figure [4] describes the bias configuration required to implement the gated configuration.

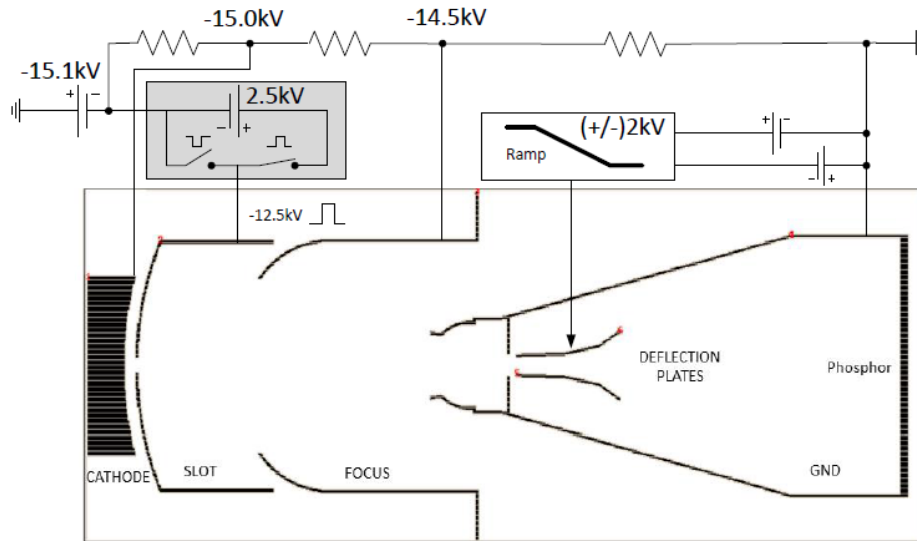


Figure [4] describes the DC bias configuration when the tube is operated in the gated mode. In this arrangement the (+2.5kV) supply floats on the (-15.1kV) supply, forcing a differential voltage of 100 Volts lower than the cathode potential preventing electrons to flow. To extract electrons, the (+2.5kV) supply is pulsed ON providing a potential difference of (2.4kV) between the slot and the cathode.

2. PRINCIPLES OF OPERATION

2.1 Overview of the electronic circuitry for gated capability

The schematic in figure [5] describes the circuitry of the stacked “Push-Pull” MOSFET configuration^{3,4} required to drive the slot voltage of the streak tube. The Push-Pull arrangement allows for symmetric rise and fall time switching in the (40-80)ns time scale depending on the load. The circuit is designed around the Cree (C2M1000170D) silicon carbide power MOSFET with $V_{ds} = 1700$ Volts and $R_{ds-ON} = 1$ Ohm. The required slot extraction voltage of ~2500 Volts requires a stack of only two MOSFETs and the Push-Pull configuration requires two additional MOSFETs totaling four for complete operation. This configuration allows only 1250 Volts across each MOSFET stage during normal operation. The arrangement of the MOSFET circuit switches the positive 2.5kV supply in series with the negative 15kV cathode supply. The tube requirement from Photonis states that for the cathode to be fully OFF (no electrons flowing), the slot (or extraction) voltage must be nominally 50-400 Volts less than (more negative) the cathode operating voltage of negative 15kV. For this configuration the OFF state of the slot voltage is required to be negative 15.1kV. The MOSFET switching is controlled by floating the entire logic group with a 15kV isolated DC-DC converter from AEB Sapphire Corporation, model XE1000-12-12S that also powers four individual gate logic supplies from Recom, model RP-1212S. The MOSFET drivers are the Intersil EL7242 operating at 12Volts. The trigger gate logic is connected to the MOSFET driver (EL7242) through the Vishay model VOW2611 opto-coupler providing 5kV isolation between each section of the MOSFET stack. This device is configured to produce logic compatible waveforms suitable for a push-pull configuration with minimal circuitry. The four opto-couplers are driven by a single buffered, fiber coupled, TTL compatible receiver (HP2416T/HFBR-24X6). For this configuration each MOSFET has a unique logic gate drive that maintains the proper gate to source voltage difference during the Push-Pull operation. A detailed single cell of the Push-Pull configuration with all the bias components is shown in figure [6].

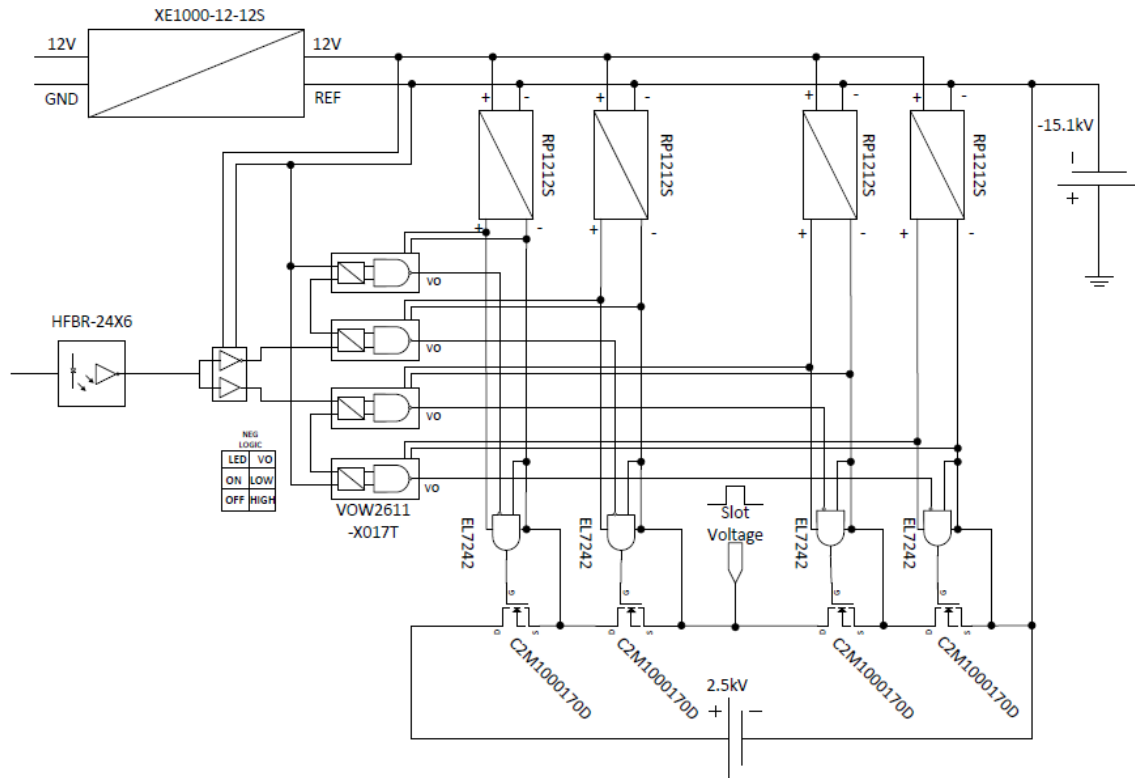


Figure [5] shows a simplified wiring diagram of the “Push-Pull” gated cathode circuit. Bias resistors and energy storage capacitors are not shown. The slot voltage is extracted from the center tap of the Push-Pull MOSFET stack arrangement. Each MOSFET has a gate driver that is powered by a floating 12 Volt supply that is referenced to the source of the MOSFET. Logic control is also referenced to the same source connection of the MOSFET maintaining the desired gate voltage with respect to the source.

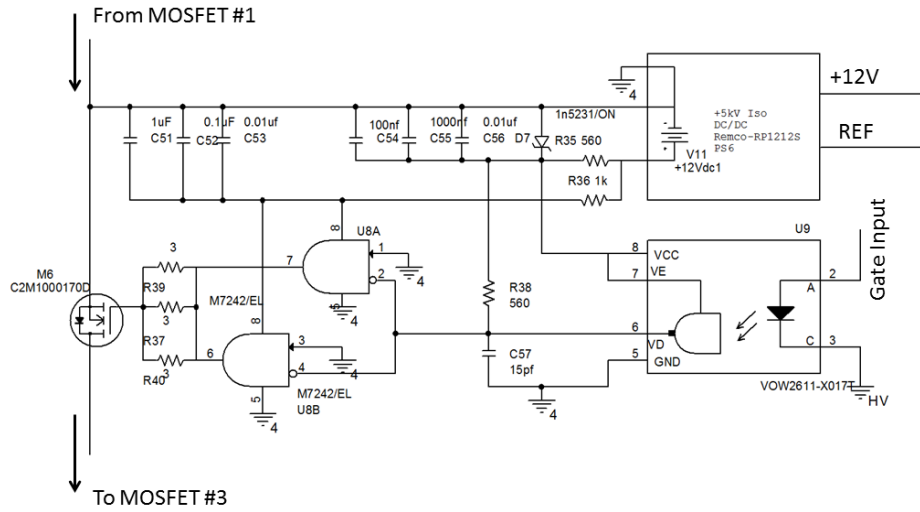


Figure [6] is a complete schematic of one of the stacked MOSFET drivers. Each MOSFET is supported by an EL7242 MOSFET driver, a VOW2611-X017T opto-coupler, and an isolated 12 Volt DC-DC converter. A 5 Volt Zener reference, model 1N5231 has been added on the isolation side of the DC-DC converter to power the opto-coupler gate.

The timing diagram is shown in Figure [7]. The trigger is initiated by an external pulse with a pulse width defining the gate ON time of the cathode. The MOSFET stack is turned ON and OFF in a complementary manner. The MOSFET stack in Group A (two of four) is turned ON and simultaneously the stack in Group B (two of four) is turned OFF. When the gate is turned OFF, the reverse is true. The switching times are determined by the rate at which the gates of the MOSFET can be charged and discharged. R_{ds} (ON) of the device and the associated capacitance of cathode connection determine the charge and discharge times. The Cree device was chosen because of the R_{ds} (ON) value (~ 1 Ohm) and the low gate to source capacitance of $C_{iss} \sim 191$ pF.

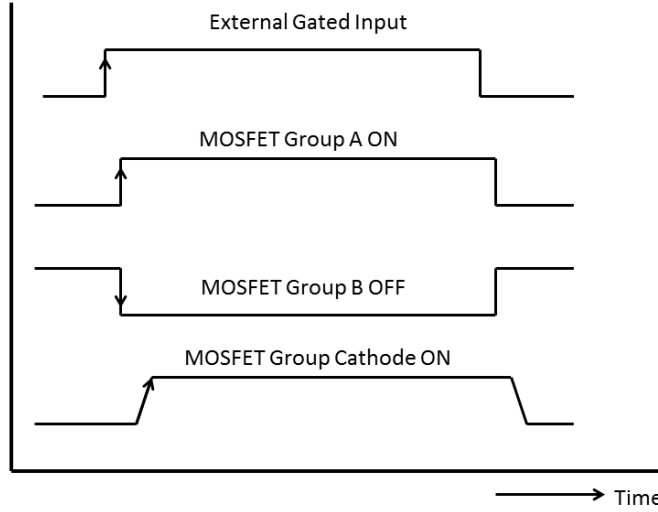


Figure [7] is the MOSFET stack timing diagram for the gated photocathode. The rise time of the cathode gate is determined by the charge time of the MOSFET gate input capacitance (C_{iss}) 191pF). This is also true for the fall time of the cathode gate. When the cathode is turned OFF, the MOSFETs in Group A goes to high impedance, when switched OFF, and the MOSFETs in Group B are switched ON. This push-pull action snaps the cathode voltage back to the voltage required to prevent electron flow between the cathode and the slot of the streak tube.

2.2 Prototype circuit performance

A double sided prototype board was fabricated and tested with a capacitive load that mimics the streak tube slot capacitance of approximately 2pF at the end of a 16 inch HV cable. In this configuration each gate was driven by external O/Es and the 2.5kV slot voltage supply was referenced to earth ground, in that the negative 15kV supply was not turned on but connected. Figure [8] describes the typical waveforms with this configuration. The measured rise and fall times of the slot voltage were limited by the cable length of the slot connection, the high voltage scope probes and the inductance of the layout and interconnections.

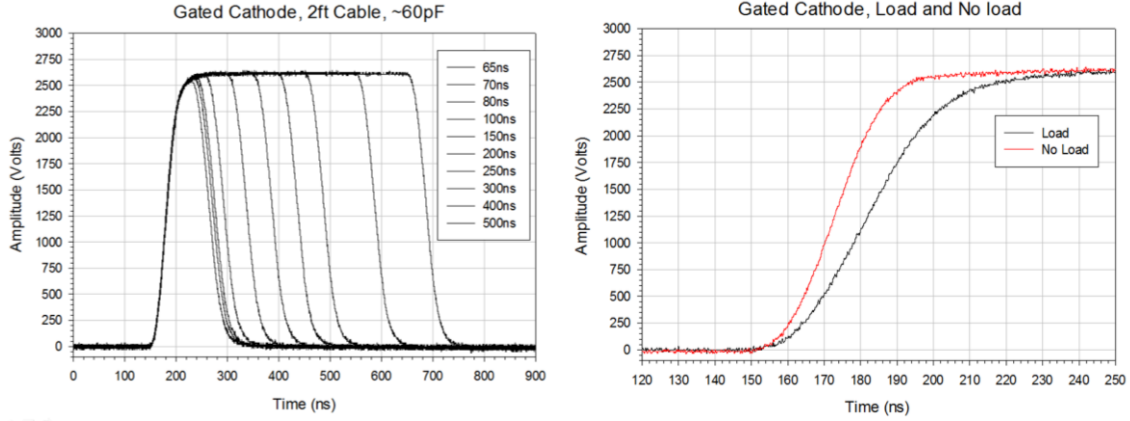


Figure [8]. The left figure describes the continuous variation of the slot voltage gate action of the Push-Pull configuration. This data was acquired using a 2ft cable with a capacitive load. The right figure describes the rise time with no load and a load that includes the cable and nominal tube capacitance. The final performance is eventually determined by the load capacitance and cable lengths.

2.3 System operation

The gated cathode configuration defines the extraction energy of the electrons when the gate voltage is applied to the extraction slot electrode. The gated cathode implementation requires specific timing considerations to prevent acquiring data during the rise and fall times of the gate. The initiation of the sweep and acquisition of data during the transitions will corrupt the data because the bias voltage for the focus setting is tuned to one electron energy. During the rise and fall times of the slot voltage, all electron energies up to the maximum energy corresponding to when the slot voltage is at the flat top of the pulse will be collected. Figure [9] illustrates this type of behavior between the gate transitions and electron energies⁵.

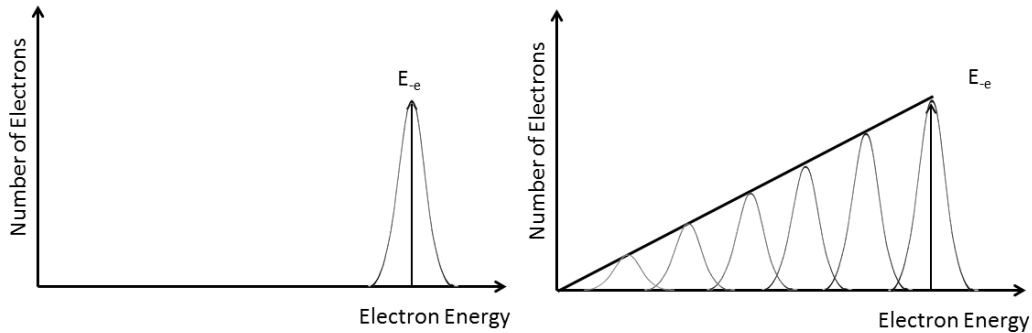


Figure [9] illustrates the electron energy distribution during transitions of the gated slot pulse. The left figure shows a normal energy distribution when operating the slot voltage in a DC mode. The electron energies are considered mono-energetic and will have a mean value (E_e). The width of energies about the mean value represents the variation of electron energies emanating from the photocathode due to thermal noise and depth of extraction. The right figure shows the allowed energies during a transition when the gate voltage varies from the OFF state to the maximum value of the slot voltage. The focus voltage is optimized for only one energy (E_e) which occurs on the flat top of the gate voltage. The sweep ramp must be applied after the transition of the gate voltage and must end before the voltage is turned off. This requirement also places a specification on the stability of the flat top of the pulse.

To avoid this type of data corruption, there must be a unique sequence of events that are to be followed. During the initiation of the gate, the sweep ramp is at the rail and the electron beam is propagating to the beam dump. When the slot voltage is stable, the application of the sweep can occur. When the sweep ramp is complete and at the other rail, the gate can be closed and because the electron beam is at the beam dump no corrupted data is recorded. Figure [10] describes the sequence of events for data to be acquired.

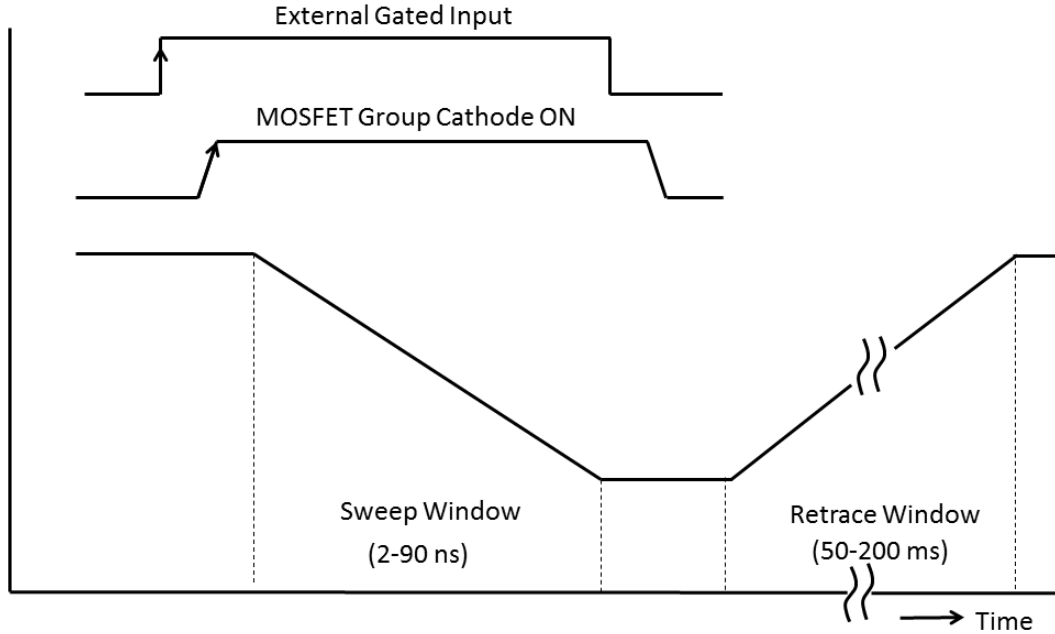


Figure [10] describing the proper sequence of gate and sweep voltages that must be followed in order to acquire a streaked image that is not corrupted by the transition edges of the gated slot voltage.

2.4 Profile measurements

Measurements of the gate profile using a 10ns pulse laser applied to the photocathode have been completed with reduced voltage settings to allow the system to operate without potting the voltage supplies that would allow operation at a negative 15kV. Potting would also prevent access to the components during testing. The voltages for this test were negative 3664 Volts on the photocathode and a pulsed slot extraction voltage of negative 3225 Volts. The focus voltage of negative 3550 Volts was selected based on the electron trajectories model such that the electrons could propagate to the anode without clipping and is not optimized for best focus at the anode². The sweep plates were held at 0 Volts. Figure [11] represent the calculated expected electron trajectories for this configuration.

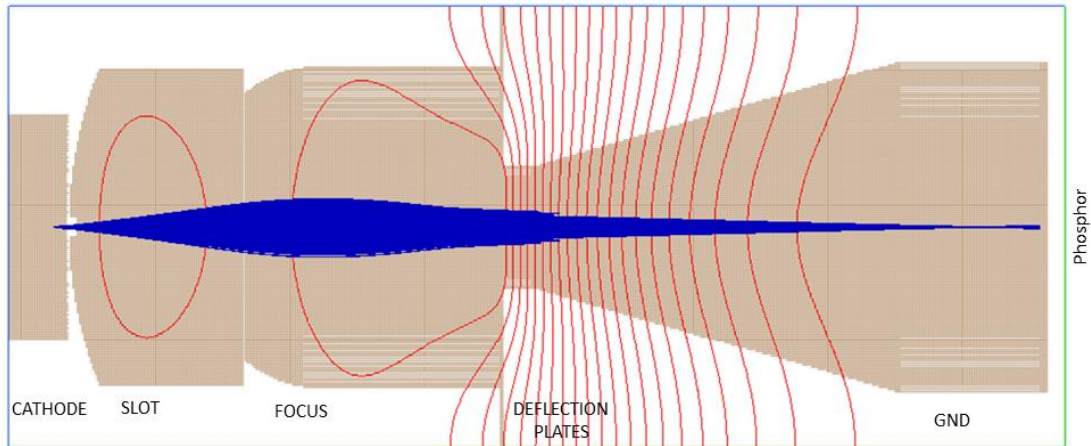


Figure [11] represents the calculated electron trajectories for the low voltage settings. The gate pulse test was completed at low voltage to prevent potting the high voltage circuitry allowing access to components with conventional probing techniques.

The measured gate profile is compared with the slot extraction pulse in figure [12]. The plot is a measurement of the light throughput prior to, during and after the gate was applied. The laser light used for the test was a 10ns HeNe laser scanned in 10ns increments along the width of the gate. During the application of the pulse it is important to have all voltages that control the tube as stable as possible. The ripple on the flat top of the pulse is related to the inductive coupling associated with the layout of the prototype hardware. It is expected to be reduced once the system is implemented in a proper assembly.

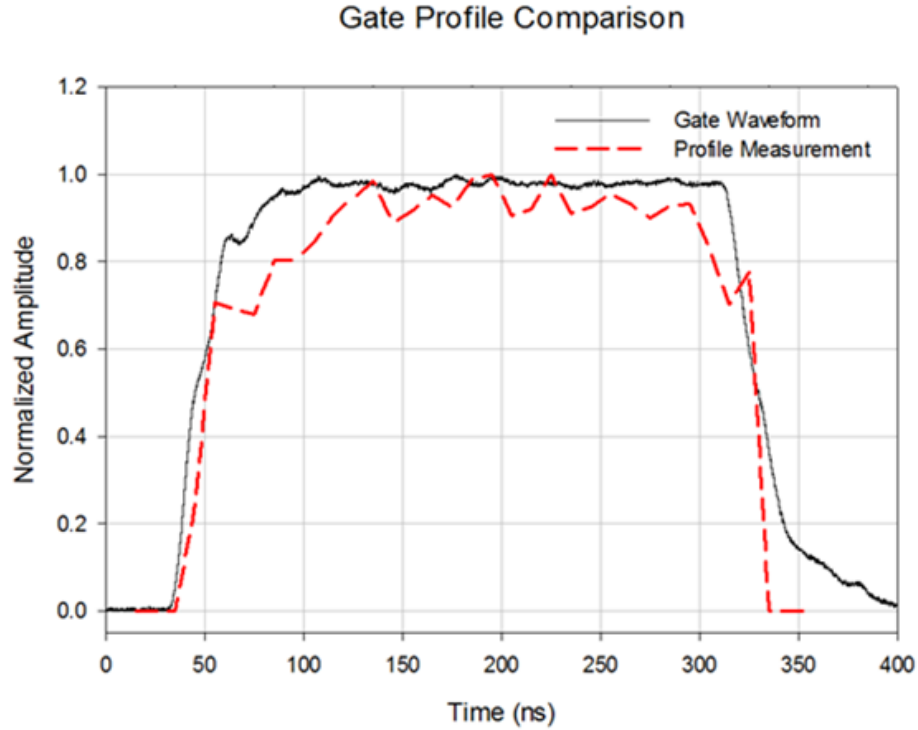


Figure [12] is a normalized measurement of the gate profile using a 10ns laser pulse that is scanned along the width of the gate set to 300ns. The voltages for this scan are Cathode (-3664V), Focus (-3550V), Slot ON (-3225V), and Slot OFF (-3861V). The profile measurement agrees with the gate width of the slot extraction pulse shape.

An additional measurement described in figure [13] is a measure of the system output in response to the application of the gate while light of constant intensity is present on the photocathode. A HeNe laser was applied to the photocathode with a pulse width much larger than the maximum desired gate width. Each sample point represents a different gate width for the same intensity of DC light. The expected results show that the intensity is proportional to the applied gate width and confirms the gate is functioning as desired.

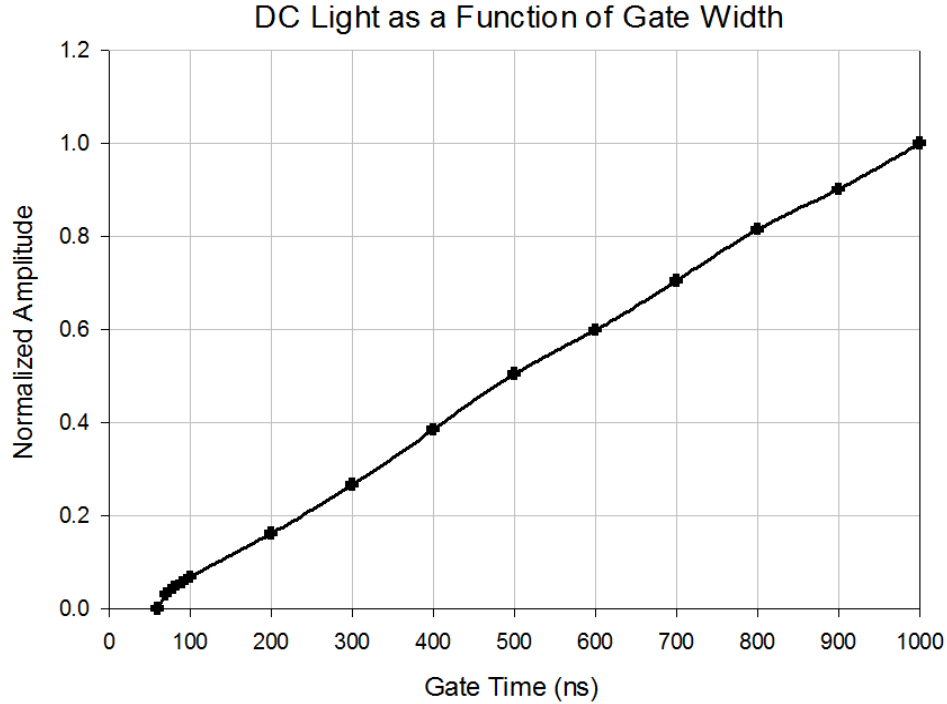


Figure [13] is a plot of the varying gate widths to a DC HeNe light source on the photocathode. A light source continuously illuminated the photocathode and images were acquired for differing gate widths. The signal drops off rapidly at the nominal 50ns gate width, and represents the rise and fall times of the gate.

3. SUMMARY

We have shown the feasibility of operating a sealed electron tube in gated mode by pulsing the slot (extraction) voltage. The configuration has been applied to the Photonis P510 tube and other tubes of similar construction can be operated with similar results. Special considerations must be followed to account for the electron energy variations during the gate transitions. For proper operation, the sweep ramp must be applied following the transition from the OFF state to the ON state and the sweep ramp must end prior to the ON state to OFF state transition.

The continuation of this effort will be to fabricate this circuit with the ability to operate the system at negative 15kV and evaluate the operation at full operating voltage. A complete evaluation of the tube performance will be conducted followed by integration into an experiment at the NIF.

ACKNOWLEDGEMENTS

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